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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/862,984	05/22/2001	Jonathan Abela	00-GR2-031	7518

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EXAMINER	
COLEMAN, WILLIAM D	
ART UNIT	**PAPER NUMBER**
2823	

DATE MAILED: 11/12/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/862,984	ABELA ET AL.	
	Examiner	Art Unit	
	W. David Coleman	2823	

-- The MAILING DATE of this communicati n appears on the cov r sheet with th correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 September 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9 and 18-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9,18-25,27 and 28* is/are rejected.

7)☒ Claim(s) *26* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Response to Arguments

Applicant's arguments with respect to claims 1-9 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-7 and 18-28 are rejected under 35 U.S.C. 102(b) as being anticipated by Charoensakvirochana et al U.S. Patent 4,644,384.

3. Pertaining to claim 1, Charoensakvirochana discloses a semiconductor apparatus as claimed. See **FIG. 5** where Charoensakvirochana teaches an injection mold **40** for encapsulating an integrated circuit chip **12** in an encapsulation material so as to form a semiconductor package containing the chip, said injection mold comprising:

at least one injection cavity **48** defined by a wall, the injection cavity being able to house the chip and receive the encapsulation material so as to encapsulate the chip in a block of the encapsulation material; and

an insert having a front part that forms a first portion of the wall of the injection cavity and a transverse surface that lies parallel to one face of the chip, wherein the transverse surface of the insert has a roughness **28** that is chosen such that the face of the semiconductor package

has a suitable roughness in a region corresponding to the transverse surface of the insert (i.e., window, which is made of quartz glass).

4. Pertaining to claim 2, Charoensakvirochana teaches the injection mold according to claim 1, wherein the insert protrudes into the interior of the injection cavity so as to form a hollow (the hollow is seen as part of the plastic housing) in the package in the region corresponding to the transverse surface of the insert.

5. Pertaining to claim 3, Charoensakvirochana teaches the injection mold according to claim 2, further comprising a blind annular space around at least a part of the insert, the blind annular space emerging in the injection cavity.

6. Pertaining to claim 4, Charoensakvirochana teaches the injection mold according to claim 1, wherein the front part of the insert has a protruding transverse surface surrounded by an annular shoulder that is set back with respect to the protruding transverse surface (the same elements of claim 3 are applied).

7. Pertaining to claim 5, Charoensakvirochana teaches the injection mold according to claim 4, further comprising a blind annular space around at least a part of the insert that emerges in the injection cavity (the blind annular space is above semiconductor die **12**).

8. Pertaining to claim 6, Charoensakvirochana teaches the injection mold according to claim 1, further comprising a blind annular space around at least a part of the insert that emerges in the injection cavity.

9. Pertaining to claim 7, Charoensakvirochana teaches the injection mold according to claim 6, wherein the annular space is enlarged in a part remote from the injection cavity.

10. Pertaining to claim 18, Charoensakvirochana teaches the injection mold according to claim 1, further comprising a first part that forms a second portion of the wall of the injection cavity, the first part having a passage in which the insert is fixed such that the front part of the insert forms the first portion of the wall of the injection cavity.

11. Pertaining to claim 19, Charoensakvirochana teaches the injection mold according to claim 18, further comprising a second part that forms a third portion of the wall of the injection cavity, the first and second parts having a parting line and between them defining the injection cavity.

12. Pertaining to claim 20, Charoensakvirochana teaches an injection mold for encapsulating an integrated circuit chip in an encapsulation material so as to form a semiconductor package containing the chip, said injection mold comprising: a first part and a second part having a parting line, the first part having a passage; at least one injection cavity defined between the first and second parts, the injection cavity being able to house the chip during encapsulation; and an insert fixed in the passage of the first part such that a front part of the insert forms a portion of the wall of the injection cavity, the insert having a transverse surface that lies parallel to one face of the chip, wherein the transverse surface of the insert has a roughness that is chosen such that the face of the semiconductor package has a suitable roughness in a region corresponding to the transverse surface of the insert.

13. Pertaining to claim 21, Charoensakvirochana teaches a semiconductor package formed in the injection mold according to claim 1, said semiconductor package comprising: an encapsulation block having a transverse face; and at least one integrated circuit chip contained in the encapsulation block, one face of the chip including an optical sensor and lying parallel to the transverse face of the encapsulation block, wherein the material of the encapsulation block that encapsulates the chip is transparent, and the transverse face of the encapsulation block includes a region located opposite the optical sensor that has a roughness that is less than the roughness of at least the rest of the transverse face of the encapsulation block.

14. Pertaining to claim 22, Charoensakvirochana teaches the semiconductor package according to claim 21, wherein the region at least covers the optical sensor of the chip.

15. Pertaining to claim 25, Charoensakvirochana teaches an information processing system including at least one optical semiconductor package formed in the injection mold according to claim 1, said optical semiconductor package comprising: an encapsulation block having a transverse face; and at least one integrated circuit chip contained in the encapsulation block, one face of the chip including an optical sensor and lying parallel to the transverse face of the encapsulation block, wherein the material of the encapsulation block that encapsulates the chip is transparent, and the transverse face of the encapsulation block includes a region located opposite the optical sensor that has a roughness that is less than the roughness of at least the rest of the transverse face of the encapsulation block.

Claim Rejections - 35 USC § 103

16. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

17. Claims 8, 9, 23, 24, 27 and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Charoensakvirochana et al., U.S. Patent 4,644,384 in view of Herbst, U.S. Patent 5,913,110.

18. Charoensakvirochana discloses a semiconductor process substantially as claimed.

Pertaining to claim 8, Charoensakvirochana teaches the injection mold according to claim 1, further comprising: first and second parts between which the injection cavity is defined (Charoensakvirochana teaches that the first and second parts are considered as an upper and lower part), wherein the first part carries the insert in such a way that the transverse surface of the inverse lies parallel to the parting line of the first and second parts. However, Charoensakvirochana fails to teach that the second part is provided with at least one movable demolding member opposite the insert and means for keeping the demolding member bearing on the package when the second part of the mold is separated from the first part of the mold during demolding. Herbst teaches a demolding member used in injection molding for semiconductor devices. In view of Herbst, it would have been obvious to one of ordinary skill in the art to incorporate at least one movable demolding member in the Charoensakvirochana semiconductor apparatus because demolding is required to remove the semiconductor device from the apparatus (see claim 7 of Herbst).

19. Pertaining to claim 9, Charoensakvirochana fails to teach the injection mold according to claim 8, wherein the first part of the mold includes pushers for demolding the package. Herbst teaches that a encapsulated semiconductor device is pushed for demolding packages. In view of Herbst, it would have been obvious to one of ordinary skill in the art to incorporate pushers in the demolding apparatus to remove the encapsulated semiconductor device from the injection molding apparatus (column 6, lines 5-68, i.e., the mold is pushed apart to remove the encapsulated semiconductor device).

Pertaining to claims 23, 24, 27 and 28 the combined teachings fails to disclose the surface roughness parameters as claimed. Given the teaching of the references, it would have been obvious to determine the optimum thickness, temperature as well as condition of delivery of the layers involved. See *In re Aller, Lacey and Hall* (10 USPQ 233-237) "It is not inventive to discover optimum or workable ranges by routine experimentation. Note that the specification contains no disclosure of either the critical nature of the claimed ranges or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. *In re Woodruff*, 919 f.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

Any differences in the claimed invention and the prior art may be expected to result in some differences in properties. The issue is whether the properties differ to such an extent that the difference is really unexpected. *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986)

Appellants have the burden of explaining the data in any declaration they proffer as evidence of non-obviousness. *Ex parte Ishizaka*, 24 USPQ2d 1621, 1624 (Bd. Pat. App. & Inter. 1992).

An Affidavit or declaration under 37 CFR 1.132 must compare the claimed subject matter with the closest prior art to be effective to rebut a prima facie case of obviousness. *In re Burckel*, 592 F.2d 1175, 201 USPQ 67 (CCPA 1979).

Objections

20. Claim 26 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

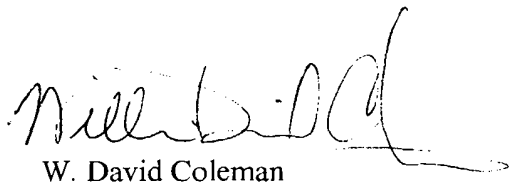
21. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

22. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

23. Any inquiry concerning this communication or earlier communications from the examiner should be directed to W. David Coleman whose telephone number is 703-305-0004. The examiner can normally be reached on 9:00 AM-5:00 PM.

24. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on 703-306-2794. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

25. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.



W. David Coleman
Primary Examiner
Art Unit 2823

WDC